JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

ANANTHAPURAMU - 515 002 (A.P.) - INDIA.

Examinations Branch

M.Tech (Seer Akademi) II Semester Regular & Supplementary September 2016 Examinations

Timetable

Time: 10:00 AM to 01:00 PM

Date / Day	Regular & Supplementary		Supplementary	
	2013, 2014 & 2015 admitted batches only		2013 admitted batches only	
	VLSI System Design (VLSISD)		Embedded Systems (ES)	
06.09.2016 Tuesday	Digital VLSI Physical Design 13J01201		Real Time Operating Systems 13J02201	
08.09.2016 Thursday	Advanced Verification using System Verilog 13J01202		Protocols & Interfaces 13J02204	
13.09.2016 Tuesday	Arm based Development 13J01203/13J02203 (Common to VLSISD & ES)			
15.09.2016 Thursday	Protocols & Interfaces 13J01204		Kernel Programming & Driver Development 13J02202	
17.09.2016 Saturday	Elective	Low Power Design for SoC 13J01205a	Elective	Hardware Software Co Design 13J02205a
		Digital Standard Cell Library Design 13J01205b		Embedded Systems Hardware Design 13J02205b
		Advanced Physical Design 13J01205c		DSP for Embedded Systems 13J02205c

Note: (i) Any omissions or clashes in this time table may please be informed to the undersigned immediately.
(ii) If any discrepancies are found, the same may be informed to the undersigned immediately.
(iii) Even if government declares holiday on any of the above dates, the examinations shall be conducted as usual.

Date: 18.08.2016

Controller of Examinations